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PATENT
Conf. No. 7959

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IN THE UNITED STATES PATENT OFFICE

Applicant: Ahmad R. Ansari et al.
Assignee: Xilinx, Inc.
Title: Method and Apparatus for Synchronized Buses
Serial No.: 10/084,569 Filing Date: 2/27/2002
Examiner: Unknown Art Unit: 2185
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PRELIMINARY AMENDMENT

Before taking action in the above-referenced case, please
make the following amendments to the claims.

IN THE CLAIMS

✓
Please add Claims 21-34 as follows:

- A1
21. (New) A system, comprising:
first and second bus masters;
first and second slaves;
a bus coupled to the first and second bus masters and the
first and second slaves; and
a bus arbiter coupled to the bus, the bus arbiter
comprising:
at least one port coupled to receive bus request
commands for a transaction from either the first or second
bus master and coupled to receive an address or identity of
the first and second slaves for the transaction, and also
coupled to communicate over the bus; and
logic circuitry that defines logic to select a bus
frequency for the requested transaction.

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02 FC:1201 168.00 CH